**We Claim:**

1. **A method** for forming microelectromechanical sensors (MEMS), wherein the sensors and the sensor signal processing electronics are monolithically integrated, comprising
   (i) firmly connecting a first silicon wafer having cavities formed thereon with a second cap wafer having an epitaxial layer by means of high temperature fusion bonding via the epitaxial layer,
   (ii) wherein the wafer composite is reduced from the second wafer towards the epitaxial layer, that is, to a membrane thickness corresponding to the micromechanical portion of the sensor or to a thickness of another portion of the semiconductor wafer responding to mechanical stress, and wherein the wafer composite is finally polished,
   (iii) wherein after the polishing process, the electronic sensor structures registered to the cavity (2a) are commonly formed along with the analogous or/and digital circuitries on the polished surface by means of CMOS technology methods.

2. The method of claim 1, characterized in that prior to the wafer bonding process, structures of electronic circuitries (4) are already on that side of the epitaxial layer (3) that faces the cavity after the bonding process.

3. The method according to claim 1 and/or 2, characterized in that the electronic structures formed on the side facing the cavity at least after the wafer bonding process extend to the polished side to form, for instance, electronically conductive channels (4a).

4. The method of claim 1, 2 and/or 3, characterized in that the electronic structures created at the side facing the cavity (2a) comprise specific sensors in particular for the analysis of the medium located adjacent to the membrane in the cavity.

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5. **A method** for forming a microelectromecanical sensor or system (MEMS), wherein at least one sensor and an associated sensor processing electronic are monolithically integrally formed,
   (i) by bonding a first wafer (2) comprising at least one cavity (2a) with a second wafer (1) carrying an epitaxial layer by means of a high temperature fusion bonding process via the epitaxial layer (3) to form a composite of the wafers;
   (ii) wherein the composite of the wafers is thinned from the second wafer down to the epitaxial layer (3) and is hereby (finally)polished;
   (iii) wherein after the polishing process at least one sensor structure (5) aligned to the cavity (2a) and at least one analogous or/and digital circuit (4) on the polished surface are formed by means of a CMOS technology method.

6. The method of claim 5, wherein thinning is performed according to a membrane thickness (3a) corresponding to the micromechanical portion of the sensor (5) or according to a thickness of another portion of the semiconductor wafer that is sensitive or responsive to a mechanical stress.

7. The method of claim 5, wherein prior to the wafer bonding process electronic circuits (4) are already formed on or aligned to the side which after the bonding of the wafers (1, 2) faces the cavity or covers the cavity.

8. The method of claims 5 or 7, wherein the electronic structures formed on the side facing the cavity extend, at least after the wafer bonding process, to the polished side and on particular form electrically conductive channels (4a).

9. The method of claim 5, wherein the electronic structures located at the side facing the cavity (2a) comprise sensors for the analysis of a medium located adjacent to the membrane (3a) in the cavity.

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10. **A micromechanical sensor** or system (MEMS), wherein at least one sensor (5) and associated sensor signal processing electronics (4) are monolithically integrally formed,

(i) by bonding the first wafer (1) comprising at least one cavity to a second wafer (2) carrying an epitaxial layer by means of a high temperature fusion bonding process via the epitaxial layer (3) so as to form a composite of the wafers;

(ii) by reducing the composite of the wafers from the second wafer down to the epitaxial layer (3) and by polishing the same;

(iii) wherein a mechanical sensor structure (5) is aligned to the cavity (2a) and is commonly provided with an analogous or/and digital circuit (4) on the polished surface at least partially in the thinned epitaxial layer (3a), formed prior to or after the polishing process by means of a monolithic integrating technology method.

11. The sensor of claim 10, wherein the thinning is performed to obtain the thickness of a membrane (3a).

12. The sensor of claim 10, wherein the circuit structure (4) is provided prior to or during the bonding.

13. The sensor of claim 10, wherein the technology method is a CMOS technique.

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